April 19, 2006

CSE2306/1308 Digital Logic

Assignment 2

Due date: Monday, May 1st

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Write your answers in the space provided in the assignment sheets.
Attach additional page if there is not enough space.
Plagiarised assignments will be given a zero mark.

Q 1: As an example of an unstructured combinational circuit design a circuit that divides a 3-bit positive binary number $a = (a_2a_1a_0)_2$ by a 2-bit positive binary number $b = (b_1b_0)_2$ calculating a 3-bit quotient $q = (q_2q_1q_0)_2$ and a 2-bit remainder $r = (r_1r_0)_2$ so that

$$\frac{a}{b} = q + \frac{r}{b}$$

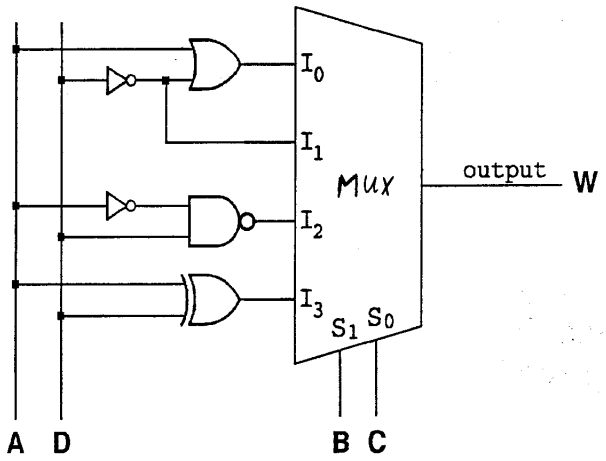
To make the task easier, take into account the following:

b	q_2	q_1	q_0	r_1	r_0
0	$-$	$-$	$-$	$-$	$-$
1	a_2	a_1	a_0	0	0
2	0	a_2	a_1	0	a_0

1. Complete the above table.
2. Derive logic equations for q and r. Aim at minimal implementation. Use Karnaugh maps when it makes the job easier.
3. Draw logic diagrams.

[4+4+4 marks]

Q 2: Consider the following logic circuit:



Complete the circuit's truth table shown below:

truth table

A	B	C	D	W
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

[6 marks]

Q 3:

A security system consists of a floodlight (**F**), a daylight detector (**D**), a motion detector for potential criminals (**C**), and a switch with four positions marked as 0,1,2,3. The switch outputs a 2-bit binary code (**A,B**) corresponding to its position.

Assume that the floodlight and detector signals are active high. Design the **minimum AND-OR logic gate circuit** that will use the switch's position to set the system's operating mode as follows:

Switch position	*Operating mode*
0	*floodlight OFF.*
1	*floodlight ON.*
2	*floodlight ON if a potential criminal and no daylight.*
3	*floodlight ON if there is no daylight.*

truth table

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

[5 marks]

Q 4: Design the logic function

$$y = f(x_3, x_2, x_1, x_0) = \sum(1, 5, 6, 8, 10, 13, 15)$$

using an 8-to-1 multiplexer.

[6 marks]

Q 5:

1. Design a 1-bit decrementer (a circuit which subtracts 1).
   Give
   (a) the arithmetic relationship between input and out put signals
   (b) the truth table,
   (c) logic diagram.

   Compare your design with that of an incrementer as presented in lecture notes.
2. Design a logic diagram of a 1-bit increment/decrement circuit controled by an id signal (increment when $id = 1$, decrement otherwise).
3. Design a block diagram of a 4-bit increment/decrement circuit.

[3+3+3+5+5 marks]

Q 6: Design a combinational circuit that **generates a sinusoid**.

The angle α will be represented as a 4-bit fraction x of $\pi/2 = 90^o$, that is

$$x = (.x_1x_2x_3x_4)_2 = \sum_{i=1}^{4} x_i \cdot 2^{-i} \quad \text{and} \quad \alpha = x\frac{\pi}{2}$$

The values of the sinusoidal function will be represented by a 3-bit fraction:

$$y = (.y_1y_2y_3)_2 = \sum_{i=1}^{3} y_i \cdot 2^{-i}$$

so that finally, we have

$$y = 2^{-3}\text{round}(7\sin(x\frac{\pi}{2}))$$

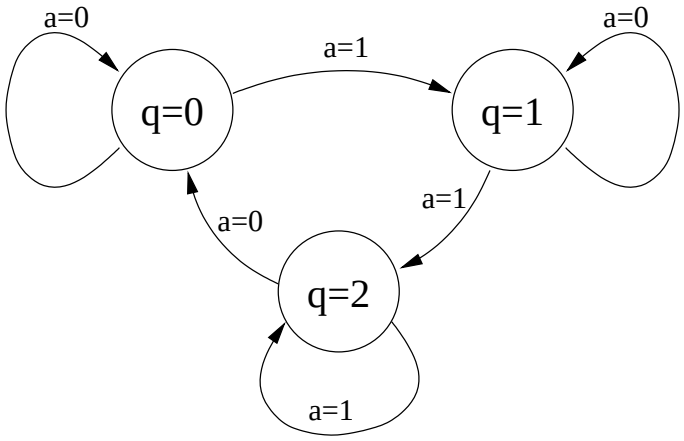
The tabular representation of the above equation is as follows:

x	y	x_1	x_2	x_3	x_4	y_1	y_2	y_3
0	0							
0.0625	0.125							
0.1250	0.125							
0.1875	0.250							
0.2500	0.375							
0.3125	0.375							
0.3750	0.500							
0.4375	0.500							
0.5000	0.625							
0.5625	0.625							
0.6250	0.750							
0.6875	0.750							
0.7500	0.750							
0.8125	0.875							
0.8750	0.875							
0.9375	0.875							

Complete the above table and derive NAND implementation of the above sinusoidal function generator.

[12 marks]

Q 7: Consider the asynchronous state machine (AsSM) described by the following **state diagram**:



where $q = (q_1 q_0)_2$

1. What is the main reason that the above AsSM will **not** work correctly? Write the answer below.

   _____

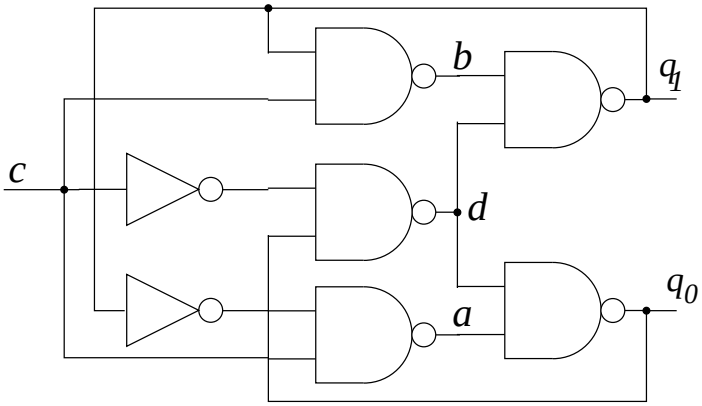
   _____

   _____

2. Modify the state diagram so that it performs the same operations and works correctly.
3. Convert the state diagram into the state table.
4. Convert the state table into the Karnaugh maps and derive the sate equations.
5. Draw the resulting logic diagram.
6. Draw timing waveforms demonstrating working of the state machine.

[2+4+3+3+4+4 marks]

Q 8: Consider the following asynchronous state machine



1. Derive the state equations.
2. Convert the state equations into the state table.
3. Convert the state table into the state diagram.
4. Draw timing waveforms demonstrating working of the state machine.

[5+5+5+5 marks]