CSE2306/1308 Digital Logic

Assignment 3

Due date: Monday, May 22

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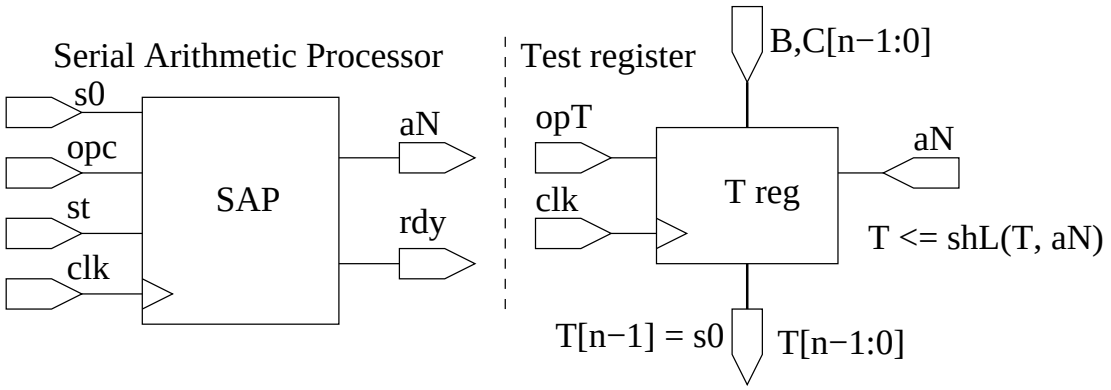
Plagiarised assignments will be given a zero mark.

This is a single question assignment worth 10 marks.

Design and test a serial arithmetic processing (SAP) unit using the FPGAdvantage tools.

- The input/output ports of the processor are as follows:



- The SAP has
  - a single 1-bit data input port, s0
  - a single 1-bit data output port, aN
  - opcode, opc , start, st , ready, rdy and clock, clk signals
- Four operations to be performed: $A <= B \left\{ \begin{array}{c} + \\ - \\ \text{AND} \\ \text{OR} \end{array} \right\} C$ selected by the opcode, opc,

  where A, B, C are 4-bit numbers
- Input and output numbers to be transferred in the most-significant-bit-first fashion.
- Assume that input numbers B, C are first loaded in a test register T from which, using the "shift left" operation, are serially shifted into SAP.

- Similarly, when the result A is formed inside SAP, it is then shifted out, most significant bit first into the test register T.
- Note that the test register should perform at least two operations: load and shL.
- The processor to be designed using the graphical entry in the FPGAdventage.

Your submission should include

- Relevant state diagrams, state tables, state equations, other logic equations,
- block and logic diagrams,
- simulation scripts,
- simulation waveforms,
- **short** description of the above.