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CSE2306 Digital Logic CSE1308

Practical 1: Introduction to HDL Designer

1.1 About this practical

In our practicals we will be using a Computer-Aid-Design package **FPGAdvantage** that consists of three main parts: the Design manager (HDL Designer), simulator (ModelSim) and a synthesizer. The objective of this practical is to introduce the Design manager (HDL Designer) that we will be using to design digital circuits and invoke simulation and synthesis tools.

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1.2 Getting started

- Create a **working directory** for all practical works. I will refer to this directory as `DigDes`.
- Create another directory `DigDes\Reports` to deposit materials related to your reports.
- Invoke **FPGAdv** tools.

  Most likely you will be able to do that from Windows **start → All Programs** menu.

  This should open **Getting Started** wizard. Select **Create a new Project** button and click **OK**
- In a **Creating a New Project** wizard specify:

  Name of new project: `P1`**you**
  Directory in which your project folder will be created: `DigDes`

  where **you** should be replaced with **your initials**.

- Click the **Next** button. This will result in a **Project Summary** window.

  If the information is correct click again the **Next** button and in the resulting **Project Content** window accept the **Create new design files** button and click the **Finish** button.

- Close the **File Creation Wizard ...** by clicking the **Cancel** button.

- Examine the **Design Manager – Project P1you** window. Inside, in the **Design Explorer** you can find one **Design Unit** , `P1you_lib`

- Set up the default parameters. In the Design Manager select **Options → Main...** to display the **Main Settings** dialog box.

- In the **General** tab set **VHDL** as the default language. All other parameters can be left with their default views.

1.3 Using Help and accessing documentation

At this stage help will be more confusing than explaining, but at some stage you might like access the following two documents that you can access from a contents page (bookcase) that pops-up when you press the **F1** function key:

- **HDL Designer Series User Manual**. Be careful the document is huge with 464 pages of information.

- **Graphical Design Tutorial** (only 234 pages!)

1.4 Create a Block Diagram

Operations performed by the HDL Designer can be invoked in a number of ways, two basic methods are from the **pull-down menus**, or selecting an appropriate button/icon. In the description I will typically refer to the pull-down menus.

- In the Design Manager select **File → New → Graphical view → Block Diagram**

  This will open a window: Untitled (Block Diagram)

- Now it is time to design your first digital/logic circuit. It will consist of just a single inverter. To do that select **Add → Component**

- It results in a **Component Browser** window. Make sure that the Library is **moduleware**.

  Select **Logic → Inverter** and drag it into the Block Diagram window. You can now close the Component Browser.

In order to complete your block diagram also known as schematic we have to add **input/output ports** and **wire** them to the inverter. We aim at obtaining the schematic as in Figure 1.
One way to proceed is as follows:

Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

Declarations
Ports:
`x : std_logic`
`y : std_logic`
Diagram Signals:

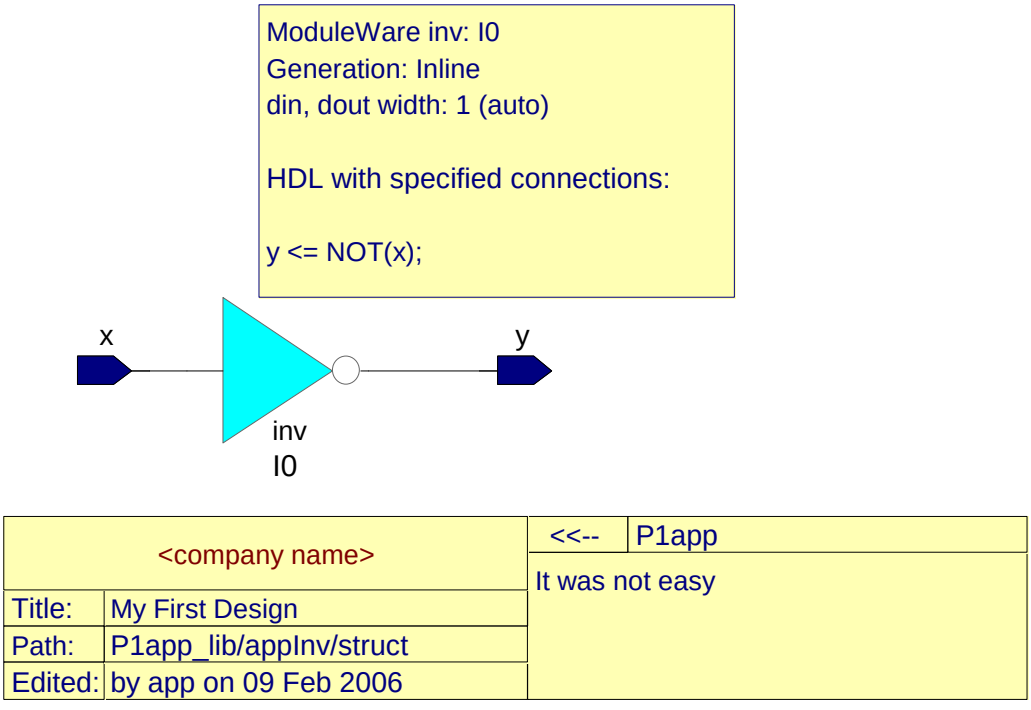

Figure 1: A complete block-diagram

- In the block diagram window select from the pull-down menu **Add → Port In**. You will now have an input port attached to the cursor the should be placed to the left of the inverter.

  Click the right mouse button (RMB) to terminate the operation.

- Similarly select **Add → Port Out** and place it to the right of the inverter.

- You have to connect ports with wires/signals to the inverter input and output respectively.

  Select **Add → Signal**. Note that the cursor now is changed to $+$. Click on two points that you are connecting.

  Remember to cancel **add signal** by clicking the RMB.

  Repeat the operation for the other port.

- Note that the ports are now associated with names `din` and `dout`, respectively. Change these names to `x` and `y`, respectively. This can be done by selecting the name and modifying the text.

1.5 Saving the block diagram

Before you do any improvements to the appearance of you schematic you should save it.

- Select **File → Save**. It will result in a dialog window **Save As Design Unit View**. In this window there are three sections: Library, Design Unit and View.
- In the Design Unit enter the name of the unit as: **you**`INV` ,
  where **you** should be replaced with your initials. Click **OK**. This results in two changes:
- The name of the Block Diagram window has been changed to
  `P1you_lib/youInv/struct`.
- In the **Design Explorer** window the component/unit `youInv` has been attached to the `P1you_lib`.
- After saving you will be able to close and restart HDL Designed without loosing your work.
  Just start again HDL Designer and in the Design explorer double click on `youInv`.

1.6 Publication of the results

The simples way to print out the block-diagram and related information is to

- select in the **Block Diagram** window **File → HTML Export ...**
- In the **HTML Export** window that appears specify the export target directory to be
  `...\DigDes\Reports`. You have created this directory at the beginning of you prac.
  You can leave all other option to their default values and click **OK**.
- It will create quite a number of files and directories in your `DigDes\Reports` directory.
  Find `P1you_libyouInvindex.htm` that you can inspect with your favourite browser.
- Find the page similar to Figure 1 and show it to the tutor.