May 11, 2006

CSE2306 Digital Logic CSE1308

Practical 10: Word-Serial Multiplication Processor

10.1 About this practical

The objective of this practical is to design and test a Word-Serial Multiplication Processor.

Contents

10.2 Introduction to the Word-Serial Multiplication Processor

The processor multiplies two 8-bit numbers and produces the 16-bit product: $P = Q \cdot D$.

Study the Lecture notes and familiarize yourself with:

- Booth's algorithm — sec. 13.1
- The top-level structure of the processor — sec. 13.2
- Datapath of the multiplication processor — sec. 13.2
- Operations of the datapath blocks — sec. 13.6
- State diagram of the control unit —- 13.4
- The structure of the control unit and VHDL program for the control unit —- 13.8

10.3 Design and test the blocks of the datapath

Design and test each block of the datapath as specified by the operation tables in sec. 13.6.

- The recommended way to proceed it to write a VHDL specification of each block/component and test its behaviour using ModelSim.

- A VHDL code for a typical register is given in sec.10.1.3. You should adopt this template for each particular code.
- The next step is to build the complete datapath: You can either
  - connect the designed blocks using graphical entry, or
  - combine VHDL specifications of individual components into one VHDL code for the complete datapath.
- Compile the VHDL code for the control unit given in sec. 13.8.

10.4 Design the control unit

The control unit is specified by VHDL code given in sec. 13.8. Compile and test its working.

10.5 The complete processor

Connect the datapath and the control unit into a complete processor.
Simulate it to obtain results similar to those in sec.13.9

10.6 The report

In your report (due after prac 8) include the results in the form of:

- Relevant state diagrams, state tables, state equations, other logic equations,
- block/logic diagrams,
- VHDL programs,
- simulation scripts,
- simulation waveforms,
- **short** description of the above.

Wherever possible publish the results selecting in the **Block Diagram** window
File → HTML Export ... . Specify the export target directory to be `...\DigDes\Reports`.