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CSE2306 Digital Logic CSE1308

Practical 2: Introduction to ModelSim simulator

2.1 About this practical

The objective of this practical is to introduce a ModelSim simulator which is a companion package to the HDL Designer. The ModelSim simulator allows you to verify if your project works according to specifications.

Contents

2.2 Creating a new project and block diagram

Follow the instructions from **prac1** to create a new project with a new block diagram that will be used in simulation.

- Start Designer Manager invoking **FPGAdv** tools.
- In the **Getting Started** wizard select **Create a new Project** button and click **OK**
- In a **Creating a New Project** wizard specify:

  Name of new project: `P2`**you**
  Directory in which your project folder will be created: `DigDes`

  where **you** should be replaced with **your initials**.
- Click the **Next** button. This will result in a **Project Summary** window.

- Set up the default parameters. In the Design Manager select **Options → Main...** to display the **Main Settings** dialog box.
- In the **General** tab set **VHDL** as the default language. All other parameters can be left with their default views.
- Open a Block Diagram window by selecting in the Design Manager
  File → New → Graphical view → Block Diagram
- Now select **Add → Component** and in a **Component Browser**, in the library **moduleware** find **Logic → N input XOR** and position it in the Block Diagram window.
- **File → Save** the diagram: in the dialog window **Save As Design Unit View** in the **Design Unit** section enter the name of the unit as: **you**`XOR` ,
  where **you** should be replaced with your initials. Click **OK**.

We aim at obtaining the diagram as in Figure 1.

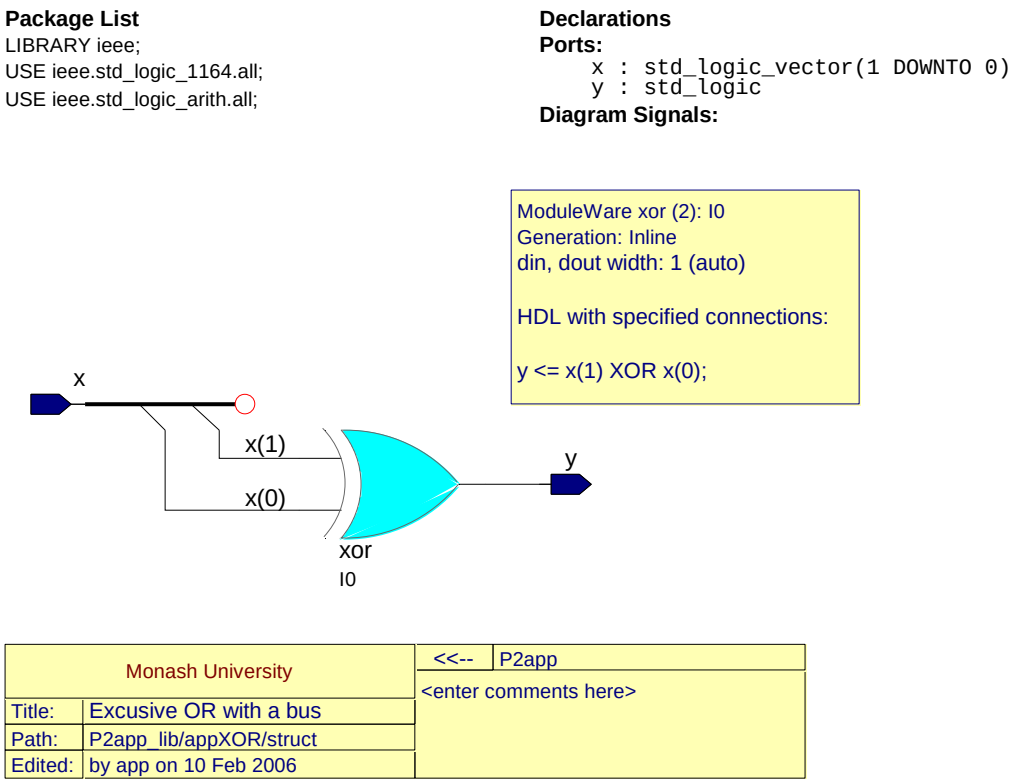

Figure 1: An exclusive-OR with a bus

2.2.1 Adding ports and wiring

A bus is a collection/vector of signals. We will group together two signals to form a bus $\mathbf{x} = [x_1,\ x_0]$. Extraction of individual signals from a bus is called 'ripping'.

The wiring can be done in a number of ways. I did it as follows:

- Select **Add → Port In** and place the port. Remember to use RMB to terminate the operation.
- Select **Add → Bus** and extend the bus from the port (single click) to a place to the left (double click) to have the dangling connector.
- Specify the size of the bus to be **(1 downto 0)** and change its name to **x** .
- Select **Add → Signal** and connect inputs of the XOR to the bus. A ripper is created automatically. You only have to specify which bus element needs to be ripped.
- Finally, create the output port.
- After moving items around you should have the diagram exactly as in Figure 1.
- Save the diagram.
- Publish the results selecting in the **Block Diagram** window **File → HTML Export ...** . Specify the export target directory to be `...\DigDes\Reports`.

2.3 Simulation

2.3.1 Starting the simulator

- To start ModelSim simulator select in the Block Diagram window **Tasks → ModelSim Flow → Run Single**
- Accept defaults in the **Start ModelSim** window clicking OK.
- If there are no errors reported in the **Log Window** there will be a new **ModeSim** window generated.
- Note also that an additional toolbar has been created at the bottom of the Block Diagram.

2.3.2 Selecting signals to view

- In the ModelSim window, in its left pane, select first an instance **you**`xor` , and then from the puul-down menu: **View → Signals**. A window **signals** is created in which all input/output signals (ports) are listed.
- In the **signals** window select **Add → Wave → Signals in design**. This opens a **wave - default** window with all signals ready to be monitored.

2.3.3 Setting/forcing input signals

- In the **signals** window click on '+' against the `x` bus to see the individual signals `x(1),x(0)`
- Select `x(1)` and then **Edit → Clock...**. A dialog window **Define Clock** pops up.
  Specify: Duty — 50[%], Period — 100[ns], FirstEdge — Falling and click OK.
- Similarly select `x(0)` and then **Edit → Clock...**.
  Define clock as: Duty — 40[%], Period — 50[ns], FirstEdge — Falling and click OK.

2.3.4 Run simulation for 300ns

Now the big moment: in the **Block Diagram** window select **Simulation → Run → For Time**.
The result displayed in the **wave - default** window should be similar to that in Figure 2.

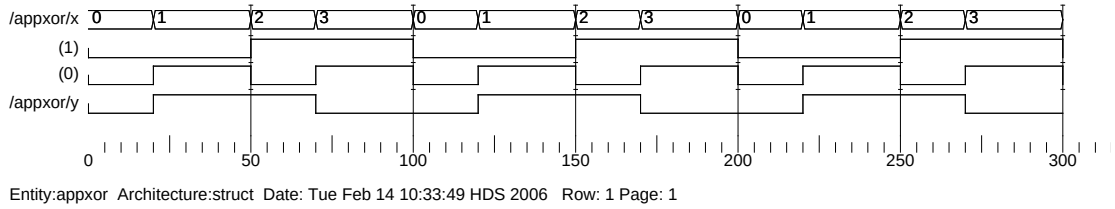

Figure 2: Simulation waveforms for an XOR gate

To achieve such results you will certainly need to restart the simulator a number of times

2.3.5 ModelSim command window

Note that all your actions have been shown in the ModelSim command window. Verify that you can simply enter a command in this window, for example **run 300**
We will use this feature to simplify our work.

2.4 Simulating NOR and NAND gates

If the time permits

- Add to your block-diagram of Figure 1 a NAND and a NOR gate.
- Simulate all three gates to obtain simulation waveforms similar to those in Figure 2, however
- modify the sequence of signals $\mathbf{x} = [x_1\ x_0]$ to be as in the Gray code, namely, 0, 1, 3, 2, 0, ...