April 5, 2006

CSE2306 Digital Logic CSE1308

Practical 6: Division-by-constant combinational circuit

6.1 About this practical

The objective of this practical is to design and test a 4-bit division-by-constant as discussed in lecture notes.

6.2 4-bit division-by-3 circuit

Design and simulate a 4-bit division-by-3 combinational circuit as described in lecture notes. Simulation results should be similar to that in Figure 1.

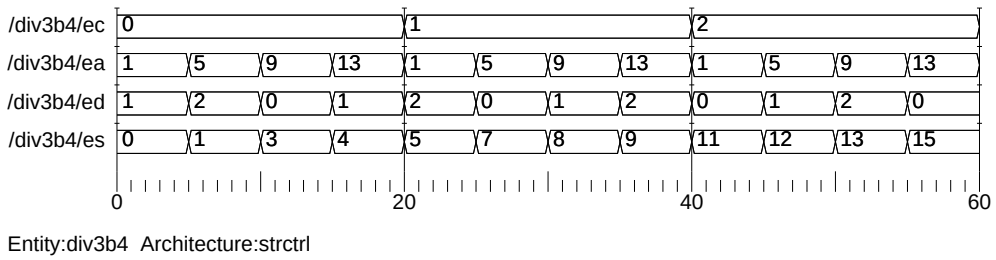

Figure 1: Simulation waveforms for a 4-bit division-by-3 combinational circut

6.3 The report

In your report (due after prac 6) include the results in the form of:

- Logic equations as specified in this manual,
- block/logic diagrams,
- VHDL programs (if available),
- simulation scripts (if available),
- simulation waveforms,
- **short** description of the above.

Wherever possible publish the results selecting in the **Block Diagram** window
File → HTML Export ... . Specify the export target directory to be `...\DigDes\Reports`.