May 1, 2006

CSE2306 Digital Logic CSE1308

Practical 8: Registers and counters

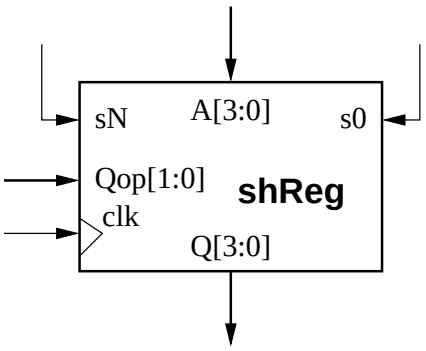
8.1 About this practical

The objective of this practical is to design and test implementation of a bi-directional shift register and an up-down counter

Contents

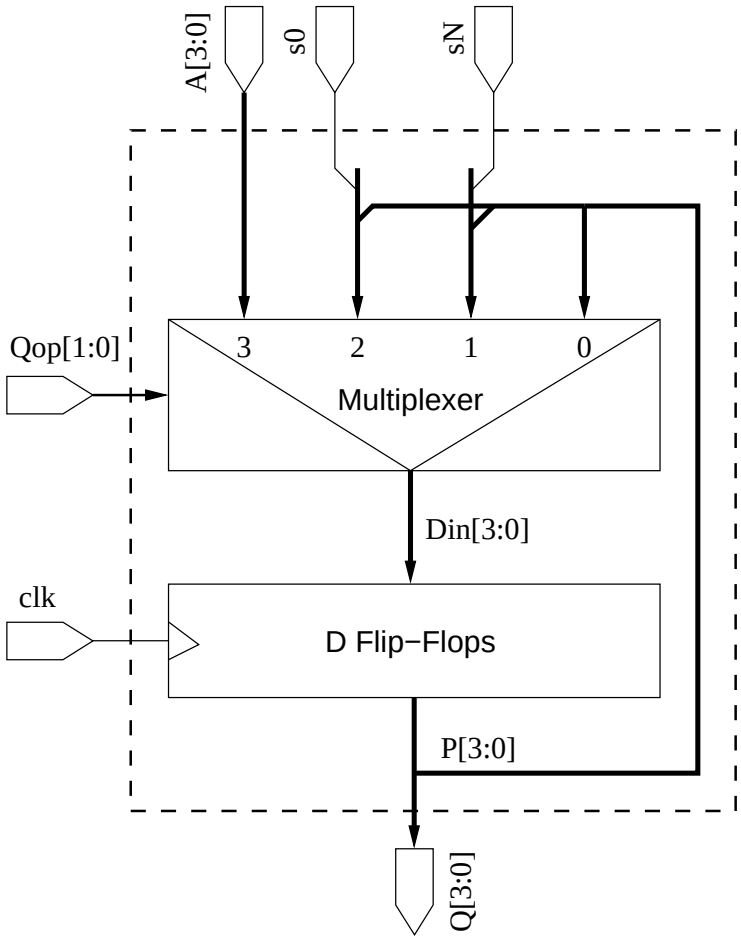
8.2 A bi-directional shift register

- Design a 4-bit bi-directional shift register as discussed in lecture notes.
- The symbol and operation table:

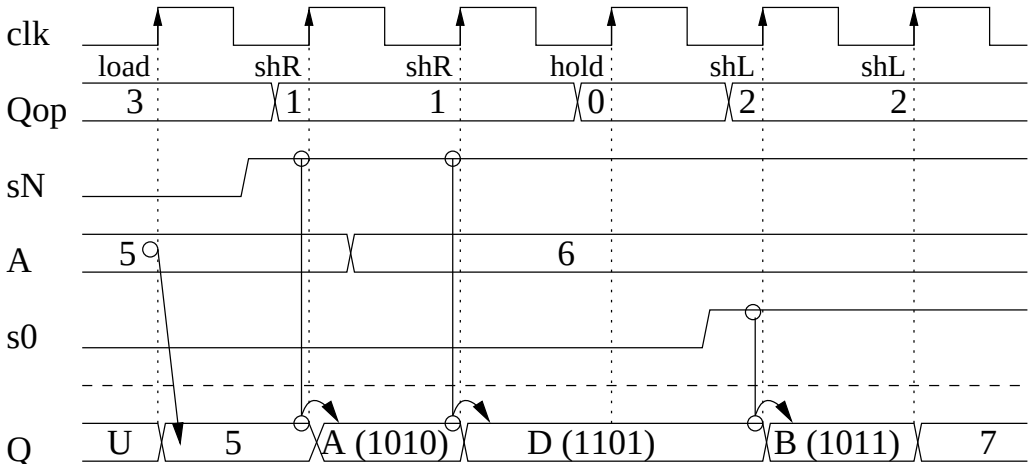


Shift register, Q		
Qop	operation	
0	Q ⇐ Q	hold
1	Q ⇐ (sN, Q[3:1])	shiftR
2	Q ⇐ (Q[2:0], s0)	shiftL
3	Q ⇐ A	load

- Use the graphical entry method and construct the following block-diagram using components from the **moduleware** library:

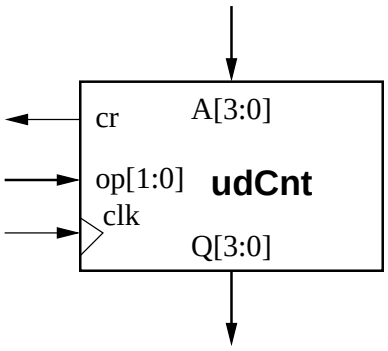


- Simulate the design. The obtained waveforms should be conceptually similar to the following:



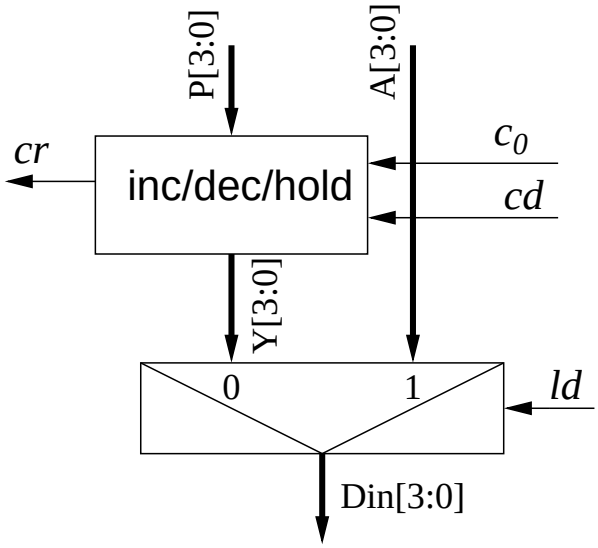
8.3 An up-down counter

- Design a 4-bit up-down counter as discussed in lecture notes.
- The symbol and operation table:

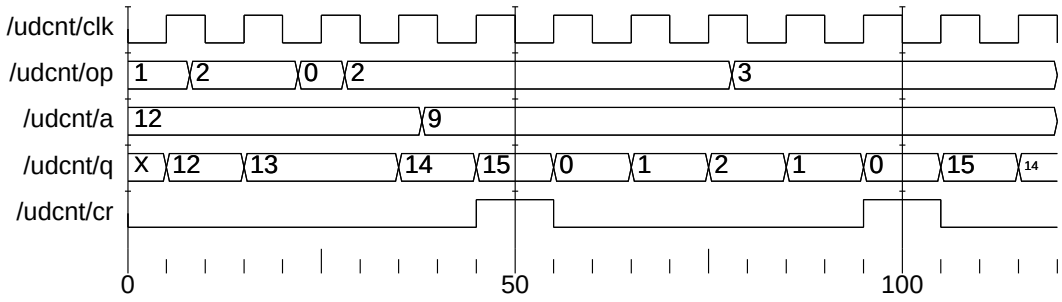


Up-down counter Q			
op	operation		cr
0	$Q \Leftarrow Q$	hold	–
1	$Q \Leftarrow A$	load	–
2	$Q \Leftarrow Q + 1$	inc	Q = max
3	$Q \Leftarrow Q - 1$	dcr	Q = min

- The block-diagram



- Use the VHDL entry method as discussed in lecture notes.
- Simulate the design. The obtained waveforms should be conceptually similar to the following:



Entity: udcnt Architecture: rtla

8.4 The report

In your report (due after prac 8) include the results in the form of:

- Relevant state diagrams, state tables, state equations, other logic equations,
- block/logic diagrams,
- VHDL programs,
- simulation scripts,
- simulation waveforms,
- **short** description of the above.

Wherever possible publish the results selecting in the **Block Diagram** window
File → **HTML Export ...** . Specify the export target directory to be `...\DigDes\Reports`.