May 7, 2006

CSE2306 Digital Logic CSE1308

Practical 9: Serial adder

9.1 About this practical

The objective of this practical is to design and test implementation of a serial adder.

Contents

9.2 A serial adder

Design and test a 4-bit serial adder as discussed in Lecture Notes.

9.3 The report

In your report (due after prac 8) include the results in the form of:

- Relevant state diagrams, state tables, state equations, other logic equations,
- block/logic diagrams,
- VHDL programs,
- simulation scripts,
- simulation waveforms,
- **short** description of the above.

Wherever possible publish the results selecting in the **Block Diagram** window
File → **HTML Export ...** . Specify the export target directory to be `...\DigDes\Reports`.