

Chapter 4

Fabrication of CMOS Integrated Circuits

4.1 Basic silicon structures

Simple Digital CMOS integrated circuits are composed of five layers of conducting materials insulated by silicon dioxide, SiO_2 , as diagrammatically shown in Figure 4.1

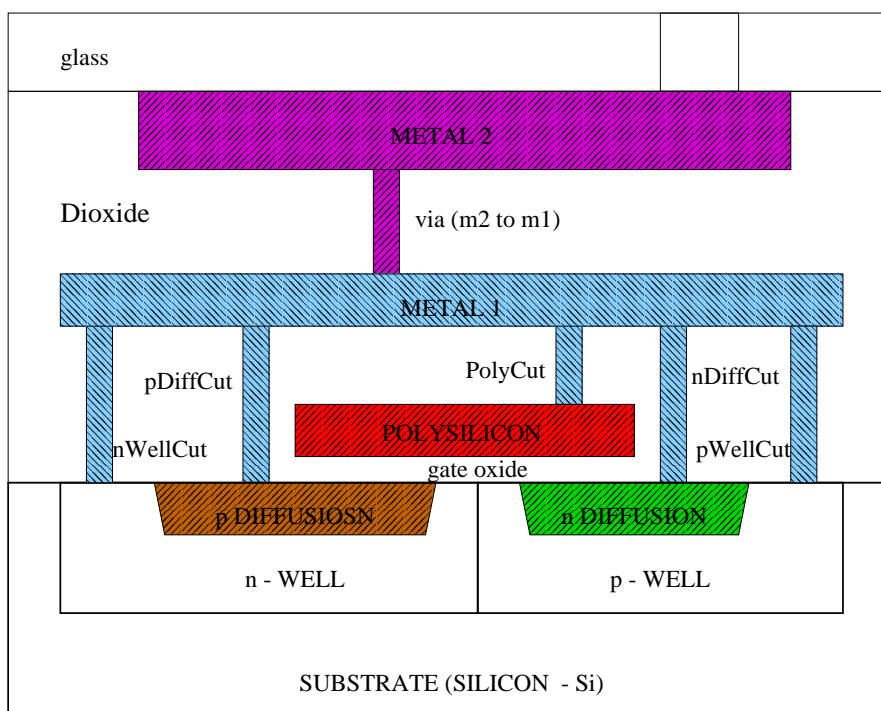


Figure 4.1: Diagrammatic cross-sectional view of a CMOS integrated circuit

The conducting material layers are as follows:

- Wells (n and p),
- Diffusion regions
- Polysilicon paths,
- Metal 1 paths,
- Metal 2 paths.

Wells For simplicity we presented a double-well structure: n-well in which pMOS transistors are fabricated, and p-well with nMOS transistors. In practice, however, we often have a single well, (say n-well) and the substrate plays the role of the opposite well.

Diffusion Note that n diffusion is created in the p-well (or p substrate) and p diffusion in the n well. Diffusion regions are also called the **active regions** and they form the sources and drains of the transistors.

Polysilicon Polysilicon paths are separated from the diffusion by a very thin layer of the gate oxide. Polysilicon forms the gates of the transistors and **short** interconnections.

Metal 1 Metal 1 layer is used to create major interconnections including the V_{DD} and the GND connections. Note that from the metal 1 the contacts are made to the wells, diffusion regions and to polysilicon layer. Such connections are made by metal filling in the cuts through the insulating silicon dioxide.

Metal 2 Metal 2 layer is used to create connections in the direction orthogonal to metal 1 paths. Note that the metal 2 layer can be connected only to the metal 1 layer through vias in the oxide. There are no direct connections possible between the metal 2 layer and layers below the metal 1, say polysilicon.

Contacts Note that we have six different types of contacts marked in Figure 4.1 as:

- **pDiffCut, nDiffCut** between diffusion regions and metal 1,
- **pWellCut, nWellCut** between wells (substrate) and metal 1,
- **PolyCut** between polysilicon and metal 1,
- **via** between metal 1 and metal 2.

Finally, in Figure 4.1, it is shown that the whole chip structure is insulated by a layer of glass with openings to solder in wires forming the external connectors.