Chapter 9

Design Examples

9.1 Design Styles for Integrated Circuits

In sec. 1.1.3 we considered two basic technologies used to build digital devices, namely, the Field Programmable Gate Arrays (FPGA), and the Application Specific Integrated Circuits (ASIC). The FPGAs are hugely successful in implementation of digital algorithms, particularly in prototyping stage, due to their programmability, they are however beyond the scope of this text. Here we consider the following design style methodologies:

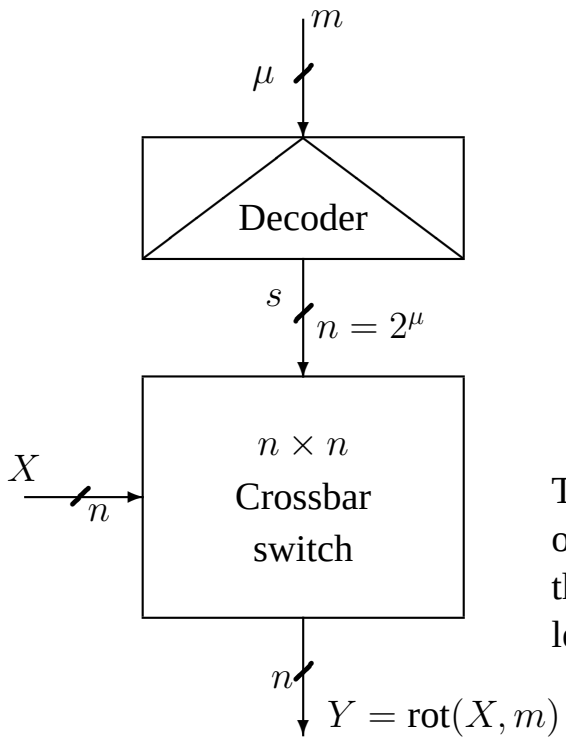
- Full-custom design style
- Standard Cell,
- Customised Gate Array.

Full-custom design method is the most time consuming and requires a significant design expertise. It is often used when the layout of the integrated circuit must be highly optimised, typically when the circuit structure is based on a two-dimensional array of identical cells. Typical examples include:

- memories,
- (multi-port) register files,
- word-parallel multiplication and similar arithmetic circuits,
- variable shifters/rotators discussed below, and others.

9.1.1 Full-custom design of a barrel shifter/rotator

A **barrel shifter/rotator** consists of a **decoder** and a **crossbar switch**, and contains two types of inputs:



- The μ-bit input m which specifies the size of the shift. The **decoder**, generates a $n = 2^{\mu}$-bit word consisting a single one at the position m.
- The n-bit input X to be shifted or rotated by the crossbar switch.

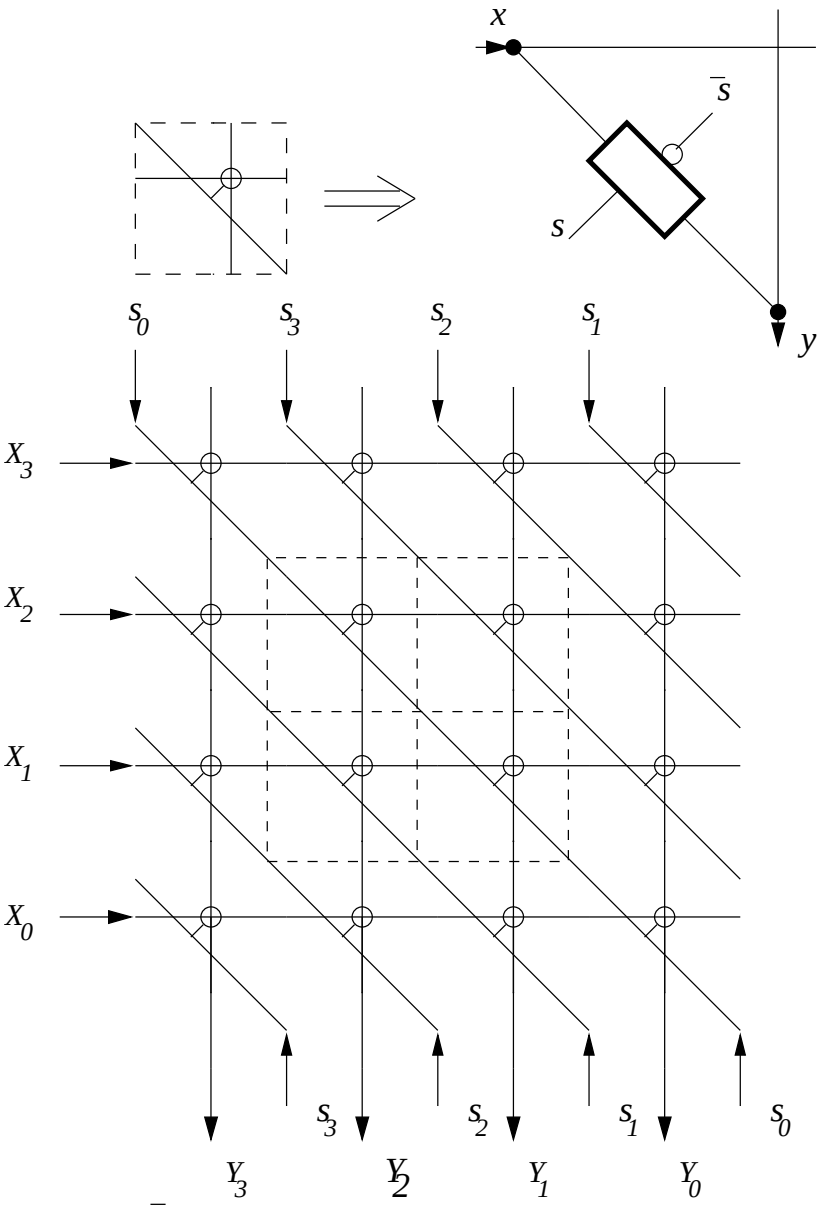
The rotator generates the n-bit output word Y which is equal to the n-bit input word, X, rotated left by m positions.

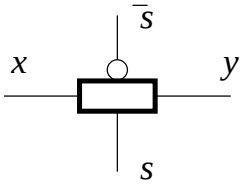
For example, for $n = 4$ ($\mu = 2$) and $m = 2$, we have

$$\begin{array}{rcccc} & 3 & 2 & 1 & 0 \\ X_{3:0} & = & [x_3 & x_2 & x_1 & x_0] \\ Y_{3:0} & = & [x_1 & x_0 & x_3 & x_2] \end{array}$$

The **crossbar switch** is a circuit which can connect every input to every output. There are $n \times n$ such connections possible, each is controlled by a switch. The switch is ideally a transmission gate, or, for simplicity a single transistor.

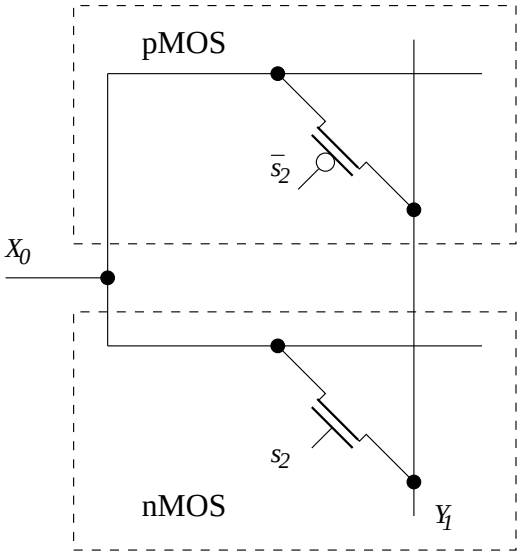
For $n = 4$ the 4×4 crossbar switch implemented using the transmission gates has the following structure:



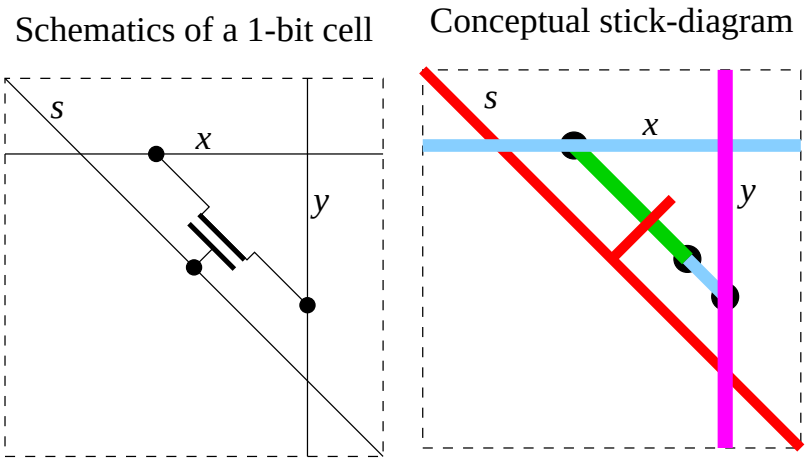


A transmission gate
(complementary switch)

If the transmission gates (a parallel connection of a pMOS–nMOS pair) are used as switches the shifter consists of two complementary sections connected in parallel, each section implemented in its respective well:

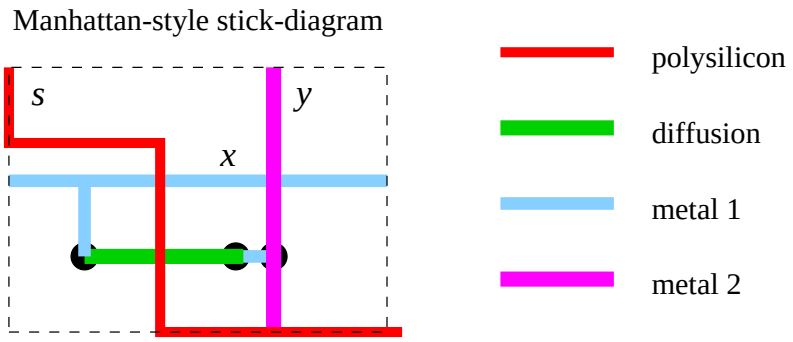


A basic building block of the crossbar switch is a 1-bit (half-)cell of the following structure:

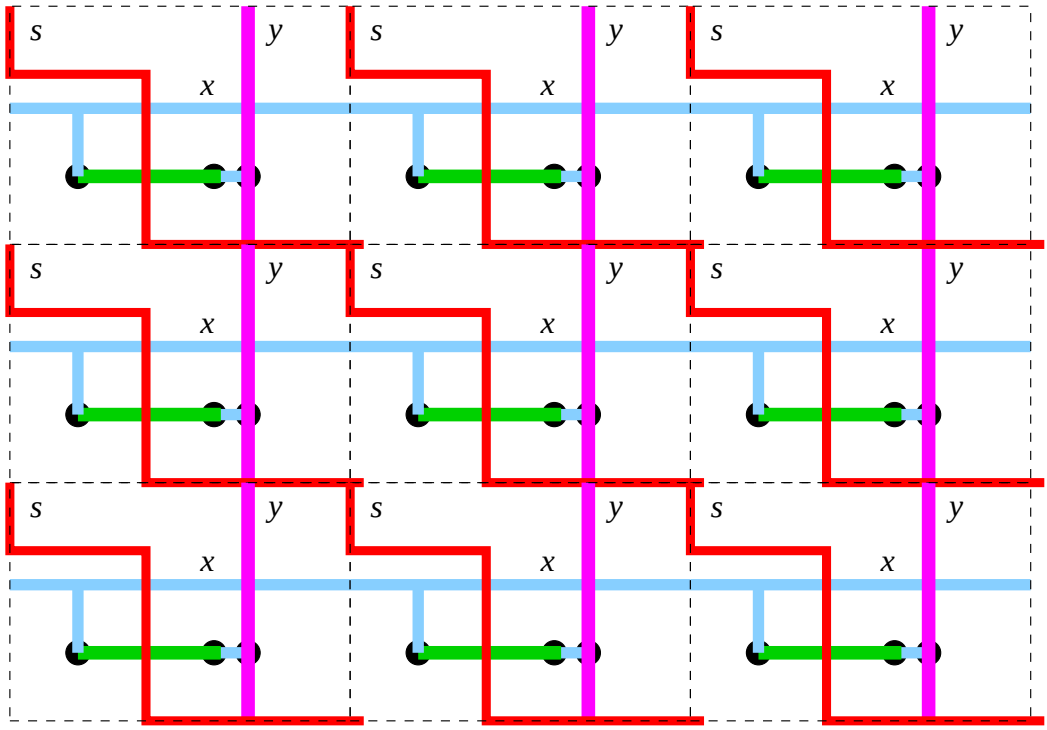


Note the metal1 input lines, metal2 output lines and polysilicon select lines driving the gates of the transistors.

Typically, only the Manhattan geometry is supported in mask layouts which requires the relevant modification of the topology of the layout:



Using the above 1-bit cell we can easily tile $n \times n$ crossbar switch as in the following example:



Finally, we have to remember to connect the well to either VDD or GND.

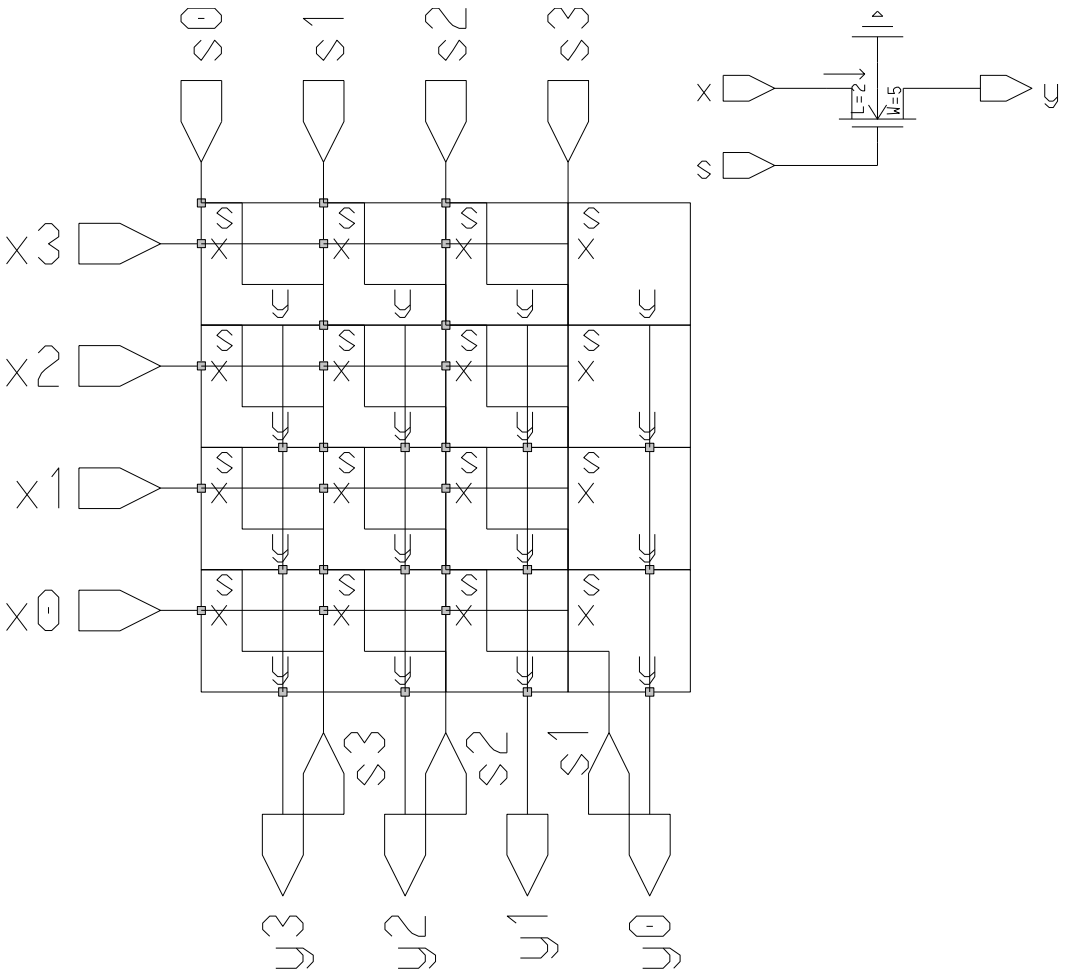
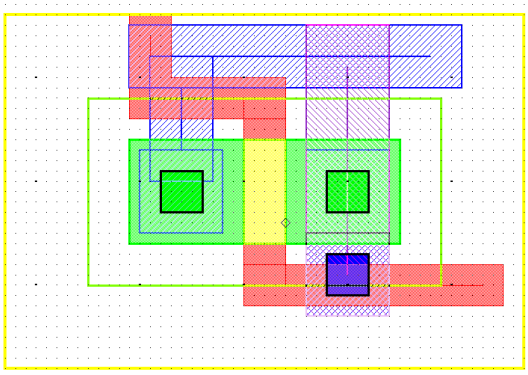


Figure 9.1: Mentor Graphics schematics of a 4×4 crossbar switch and its 1-bit nMOS components



The layout of the 1-bit component

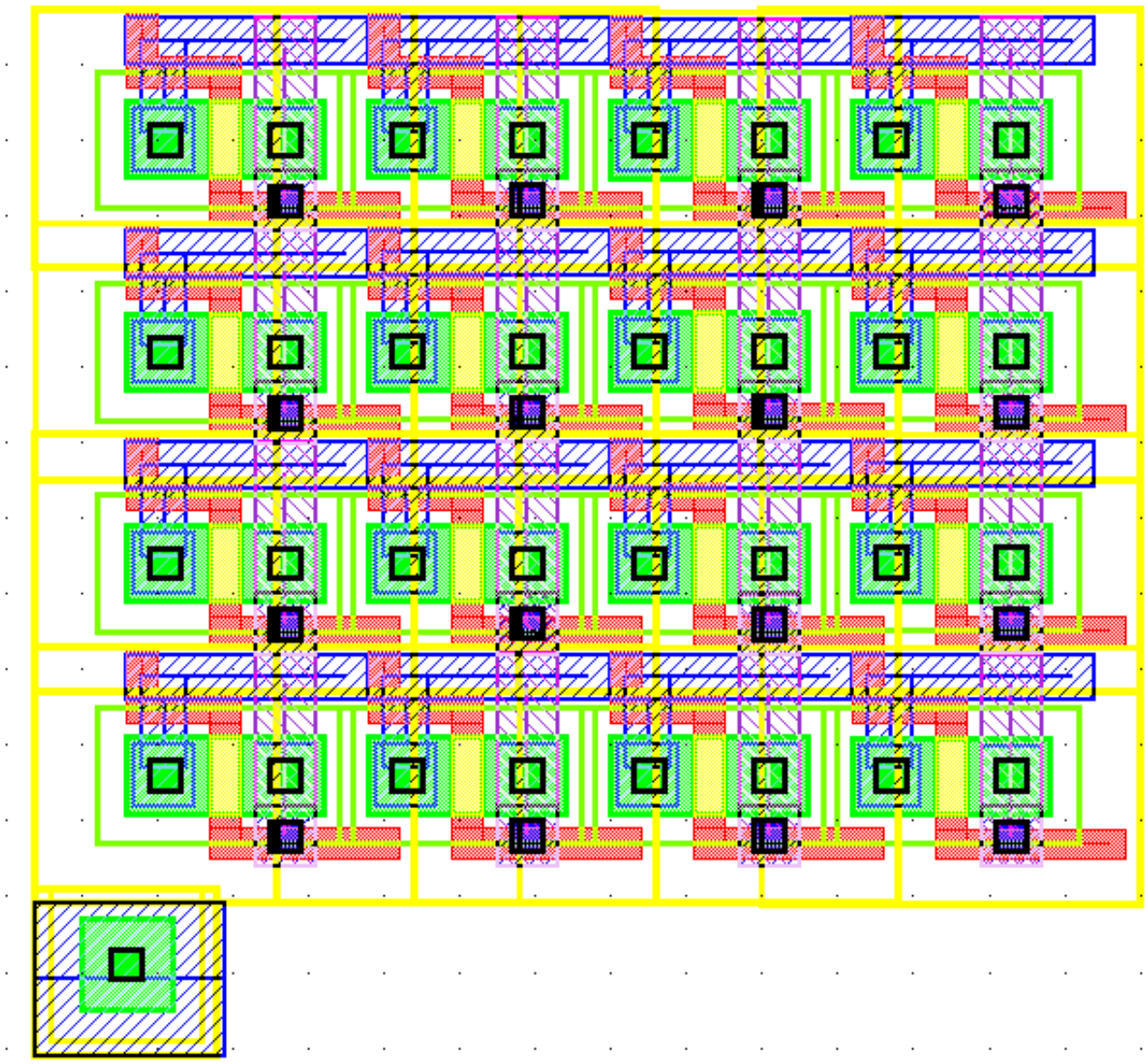


Figure 9.2: The layout of the 4×4 crossbar switch