1. Explain principles of operations of a MOS transistor.

(4 marks)

2. Describe a simplified switching model of an nMOS transistor. Give the relationship between the drain current, $I_D$, suitable voltages, transistor size, and other relevant parameters.

(4 marks)

3. Sketch and briefly explain the transfer and current characteristics of the CMOS inverter.

(4 marks)

4. Explain why in a CMOS inverter the size of the nMOS transistor is often different to the size of the complementary pMOS transistor.

(2 marks)

5. Described briefly the main technological steps required to manufacture a CMOS inverter. Clearly specify masks used in each step. Give a relevant sketch for each step.

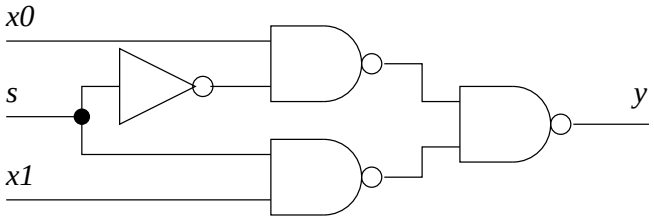
(12 marks)

6. Describe the principles of a *good layout* of a functional cell.

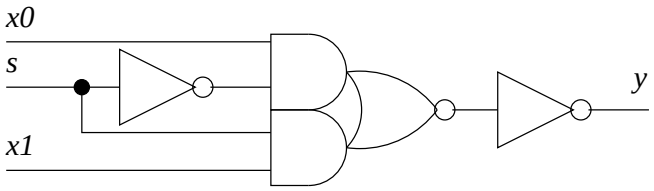
(4 marks)

7. A 2-to-1 multiplexer can be built using, at least, the following three approaches:

   (a) simple gates (e.g. NANDs):




   (b) a composite gate:




   (c) transmission gates

   For each of the above approaches draw a schematic and a corresponding stick diagram and calculate the number of transistors and contacts.

(4 + 4 + 4 = 12 marks)

8. Consider a composite gate implementation of the following logic function:

$$y = \overline{\overline{a} + \overline{b} \cdot c + b \cdot \overline{d}}$$

Draw:

(a) the transistor-level schematic of the cell.

(b) the stick diagram of the cell.

($3 + 5 = 8$ marks)

9. Compare characteristic features of the CMOS switch logic versus the gate logic.

($4$ marks)

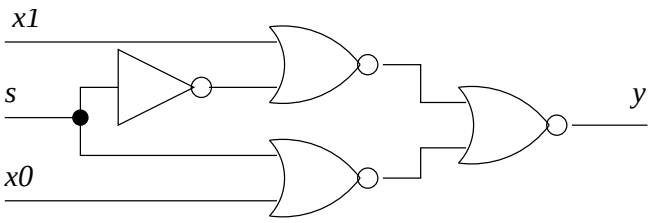
10. Compare the structure of a "weak" 2-to-1 multiplexer with its counterpart based on transmission gates. Sketch relevant schematics and stick diagrams.

($4$ marks)

11. Sketch a schematic of an XOR gate based on a "weak" multiplexer.

($4$ marks)

12. Consider the NOR-based implementation of a 2-to-1 multiplexer:

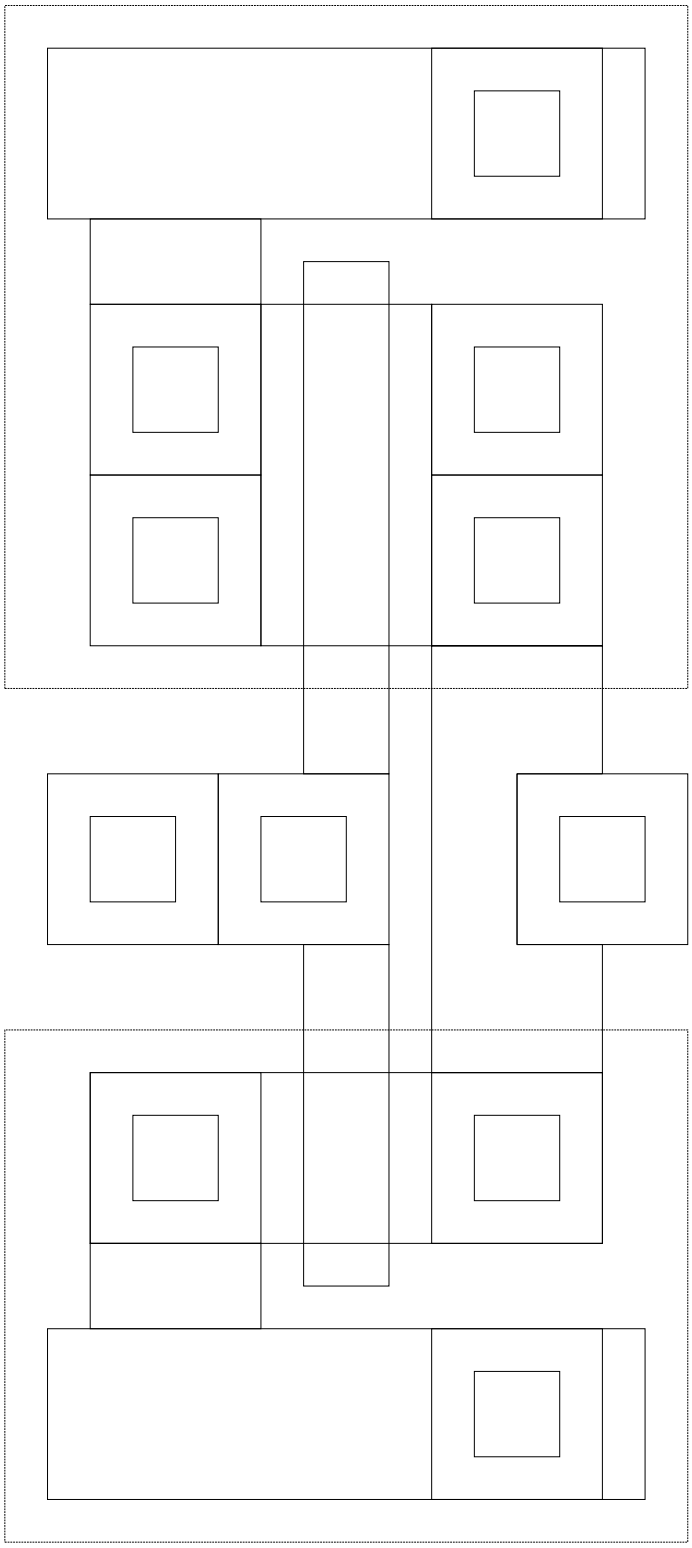



Sketch a layout of the **standard cell** implementation of the above multiplexer. Estimate the total area of the implementation assuming that the size of a NOR gate is $80 \times 40\lambda$, and an inverter — $80 \times 30\lambda$.

($6$ marks)

13. Annotate the following layout. To make the task easier you might like to colour it first. The best way to annotate the layout is to draw an arrow to every component of the layout and write a corresponding name.

(10 marks)



14. Give a top and cross-sectional views of the:

    (a) well-to-VDD/GND contact,

    (b) diffusion contact,

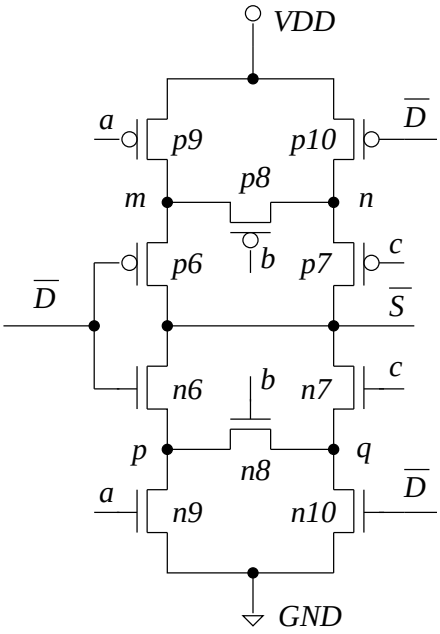
    (c) polysilicon contact.

($2 + 2 + 2 = 6$ marks)

15. Give a logic diagram, schematic and a colour stick-diagram of a D-latch implemented using **tri-state inverters**.

($10$ marks)

16. Consider the following CMOS circuit:




    (a) Derive suitable circuit graphs for the p-MOS and n-MOS section of the circuit.

    (b) Determine the degree of each node.

    (c) Find the Eulerian paths if they exist. If they do not exist, minimise the number of diffusion gaps.

    (d) Determine the layout matrix of the circuit.

    (e) Sketch the colour stick-diagram of the circuit.

($2 + 1 + 2 + 3 + 6 = 14$ marks)

17. Consider the following layout matrix:

$$\mathcal{L} = \begin{bmatrix} B & (p1) & F & (p3) & V & (p2) & E \\ & C & & G & & B & \\ B & (n1) & A\,!\,F & (n3) & G & (n2) & E \end{bmatrix}$$

Draw the corresponding

(a) stick diagram,

(b) schematic, and

(c) logic diagram.

(d) Explain the function of the circuit

($3 + 3 + 2 + 2 = 10$ marks)

18. Compare two implementations of a tri-state inverter. Sketch relevant schematics and stick diagrams.

($4$ marks)

19. Discuss in detail the major components of a tri-state output pad. Give the schematic of the driver and the protecting circuitry.

($8$ marks)

20. For a positive edge-triggered T-type flip-flop:

(a) give the state-diagram,

(b) explain how it can be implemented

($6 + 2 = 8$ marks)

21. Describe a structure a NOR-based ROM. Explain how the data is stored.

($6$ marks)

22. Describe the structure and operation a single transistor cell of a DRAM.

($6$ marks)

Marks do not add up to 100, they add up to 150 instead.